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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: **Krutko et al.**
Appl. No.: 10/783,830
Filed: February 20, 2004
TC/A.U.: 2811
Examiner: not yet assigned
Docket No.: 060999-0185
Customer No.: **009629**
For: **STRUCTURES AND METHODS FOR FABRICATING
INTEGRATED HBT/FET's AT COMPETITIVE COST**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Sir:

Pursuant to 37 C.F.R. §§ 1.56 and 1.97(b), Applicant brings to the attention of the Examiner the documents listed on the attached PTO-1449. This Information Disclosure Statement is being filed before the mailing of the first Office Action on the merits.

A copy of each listed document is attached except for U.S. Patents. Applicant respectfully requests that the Examiner consider the listed document and evidence that consideration by making appropriate notations on the attached form.

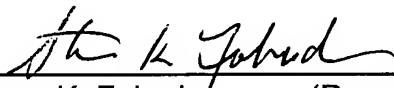
This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that the listed document is material or constitutes "prior art." If it should be determined that the listed document does not constitute "prior art" under United States law, Applicants reserve the right to present to the Office the relevant facts and law regarding the appropriate status of such document. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed document, should the document be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 50-0310.

Respectfully submitted,

Morgan, Lewis & Bockius LLP

Date: May 28, 2004



Steven K. Fukuda (Reg. No. 44,690)

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Attachments

(Use several sheets if necessary)

PTO Form 1449

Attorney Docket No.
60999-185

Serial No.	10/783,830
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Applicants

Krutko et al.

Filing Date

February 20, 2004

Group	Mean	SD	95% CI
Control	1.00	0.00	1.00
Low	1.00	0.00	1.00
High	1.00	0.00	1.00

2811

U.S. PATENT DOCUMENTS

[illegible]

FOREIGN PATENT DOCUMENTS

[illegible]

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

C01	W.J. Ho, M.F. Chang, S.M. Beccue, P.J. Zampardi, J. Yu, A. Sailer, R.L. Pierson, K.C. Wang, "A GaAs BiFET LSI technology", GaAs IC Sym. Tech. Dig., 1994, p.47.
C02	D. Cheskis, C. E. Chang, W. H. Ku, P. M. Asbeck, M.F. Chang, R.L. Pierson, S. Sailer, "Co-integration of GaAlAs/GaAs HBT's and GaAs FET's with a simple manufacturable process", IEDM Tech. Dig., 1992, p. 91.
C03	D. C. Streit, D. K. Umemoto, K. W. Kobayashi, A. K. Oki, "Monolithik HEMT-HBT integration by selective MBE". IEEE Trans. Electron Devices, vol. 42, 1995, p.618.
C04	D. C. Streit, D. K. Umemoto, J. R. Velebir, K. W. Kobayashi, A. K. Oki, "35 GHz HEMT amplifiers fabricated using integration HEMT-HBT material grown by selective MBE", IEEE Microwave Guided Wave Lett., vol. 4, 1994, p.361.
C05	K. Itakura, Y. Shimamoto, T. Ueda, S. Katsu, D. Ueda, " A GaAs Bi-FET technology for large scale integration", IEDM Tech. Dig., 1989, p. 389.

	C06	Y. F. Yang, C.C. Hsu, E.S. Yang, "Integration of GaInP/GaAs heterojunction bipolar transistors and high electron mobility transistors", IEEE Electron Device Lett., vol. 17, no. 7, July 1996, p. 363
	C07	J. H. Tsai, " Integrated fabrication of InGaP/GaAs d-doped heterojunction bipolar transistor and doped-channel field effect transistor", 2002 IEEE, p. 365.
	C08	J. Jang, E. C. Kan, T. Amborg, T. Johansson, R. Dutton, "Characterization of RF Power BJT and Improvement of Thermal Stability with Nonlinear Base Ballasting", 1998 IEE, pg. 1428.

Examiner	Date Considered
Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	